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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
RA 5487

I hereby certify that this correspondence is being faxed to the USPTO central fax number (571) 273-8300 (37 CFR 1.8(a)

on July 6, 2006

Signature Beth L. McMahon

Typed or printed name Beth L. McMahon

Application Number	Filed
10/620,515	07/16/2003

First Named Inventor
Kelvin S. Vartti

Art Unit	Examiner
2186	Lev Iwashko

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 41,987
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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07/06/2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of 3 forms are submitted. Transmittal; Notice of Appeal; Pre-Appeal Brief Request & Reasons

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Group Art Unit: 2186
Examiner: Lev Iwashko

Customer Assignment No.	027516	**July 6, 2006**
Serial No.:	10/620,515	
Filed:	7/16/2003	
In re Application of:	Vartti et al.	
Title:	Programmable System and Method for Accessing a Shared Memory	
Docket No.:	RA-5487	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Pre-Appeal Brief Request for Review – Reasons for Request

The pending Office Action finally rejects Claims 1-32.

Before considering the specific rejections, a brief summary of Applicants' invention is provided. In one embodiment, Applicants' invention relates to a system having first and second storage devices coupled to a control circuit. For instance, the first storage device may be a dedicated processor cache and the other storage device may be a cache that is shared between multiple processors. The control circuit receives requests for data. This data may be stored in one or both of the storage devices. The control circuit retrieves the requested data in a manner that is based on programmable mode indicators. For instance, in one mode, the control circuit will first attempt to retrieve the data from the first storage device. If the data cannot be obtained from this first storage device, a reference to the other storage device is initiated. In another mode, the control circuit references the second storage device to obtain the data before accessing the first storage device. In yet a different mode, the control circuit will attempt to retrieve the data from only a predetermined one of the storage devices. (Applicants' Spec. pp. 4-5.)

CERTIFICATE OF MAILING (37 CFR 1.8(a)) CERTIFICATE OF MAILING (37 CFR 1.8(a))

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Beth McMahon — July 6, 2006
(Beth McMahon)

Turning to the Claims, Claims 12-20 and 22-32 have been twice rejected under 35 USC §102(b) as being anticipated by U.S. Patent 5,627,992 to Baror.

Independent Claim 12 describes a control circuit to receive a request for data, copies of which may be resident within first memory logic and at least one other memory. The control circuit determines, based on a programmable mode indicator, whether to attempt to retrieve the requested data from the first memory, the other memory, or both.

In contrast to Applicants' Claim 12, Baror describes a cache system that may be programmed in either a write-through or a copy-back mode. When operating in a write-through mode, every write access is performed to the main memory. If a cache hit occurs, the data is also stored to the cache. (Baror col. 6 lines 25-29.) When operating in a copy-back mode, a write access is performed only in the cache in the case of a cache hit. The updated data is later copied back to main memory when a modified block is replaced. (Baror col. 4 lines 26-29.)

The Examiner cites the aspect of configuring the Baror cache according to write-though versus copy-back mode as teaching Applicants' control circuit and programmable mode of Claim 12. (Final Rejection p. 2.) However, this cited aspect of Baror relates to storing data to cache and/or memory. In contrast, Applicants' control circuit of Claim 12 describes a control circuit for retrieving requested data from one or both of two different memories based on a mode setting.

In addition to the foregoing, the Examiner cites the Baror Memory Address Logic (MAL) as teaching Applicant's first memory. (Final Rejection p. 2.) The Baror MAL is an address generator that includes two address incrementers, one for generating addresses when references are occurring to an integrated cache unit, and another for generating addresses for read operations initiated by this unit. (Baror col. 15 lines 39-44.) This Baror MAL does not teach Applicants' first memory logic of Applicants' Claim 12 from which requested data may be retrieved, as is described by Claim 12 line 11.

For at least the foregoing reasons, the rejection of independent Claim 12 based on Baror is improper. Claims 13-21 depend from independent Claim 12, and the rejection of these Claims is likewise improper.

Independent Claims 22 and 30 include aspects similar to those discussed in regards to independent Claim 12. The rejection of these Claims based on Baror is improper for reasons similar to those discussed above in regards to the rejection of Claim 12. Likewise, the rejection of dependent Claims 23-29 and 31-32 that depend from these independent Claims is improper.

Next, Claim 1 is considered. This Claim is rejected under 35 USC §103(a) as being unpatentable over U.S. Pat. No. 5,911,149 to Luan et al. ("Luan") in view of U.S. Pat. No. 6,496,277 to Chapin et al. ("Chapin").

Luan first describes a prior art data processing system shown in Figure 1A. This system includes a peripheral memory 107 provided for dedicated use by a peripheral controller 106. A second memory 104 is provided for dedicated use by a CPU 101. Luan describes this prior art system as having disadvantages, since the peripheral memory may

> "be quite large and is often times under-utilized if the peripheral associated with peripheral controller 106 does not require use of the entire memory space provided by memory 107. This under utilization of memory degrades system capability and increases the overall memory cost in a computer system." (Luan col. 1 lines 38-43.)

Instead of this prior art system, Luan proposes a system that utilizes a single programmable memory. A first portion of the memory may be programmably dedicated to use by a processor, and a second portion of the memory may be shared by the processor and any peripherals. (Luan Abstract.) This single Luan memory is implemented by memory devices 104 of Luan Fig. 2, each of which provides a portion of the memory address space. The Luan memory is programmably configured by system controller 201 and memory configuration controllers 202.

Claim 1 is similar to Claim 12 described above. It includes a first storage device and at least one additional storage device. Requested data may be stored within both of these storage devices. A control circuit is provided to

retrieve the requested data from at least one of the storage devices based on the state of programmable indicators.

The Examiner cites the **two memories** 104 and 107 **of the *prior art system*** shown in Figure 1A as teaching Applicants' first and additional storage devices, respectively. (Final Rejection p. 8.) The Examiner further cites the **memory configuration controller 202 of the Luan system** (Fig. 2) as teaching Applicants' control circuit.

As discussed above, the Luan system of Fig. 2 is specifically designed to eliminate the two dedicated memories of the Fig. 1A prior art system in favor of a single shared memory that is configurable by the memory configuration controller 202. Luan describes this improvement as being desirable because it eliminates the additional underused peripheral memory, thereby decreasing system costs. Based on this specific Luan teaching, there is absolutely no motivation to add the two dedicated prior art memories of Fig. 1A back into the Luan system of Fig. 2. In fact, doing so would defeat the very purpose of the Luan system. Additionally, if the two prior art dedicated memories are (somehow) incorporated back into the Luan system, there is no need to use the Luan memory configuration controller 202 to programmably control use of the memory, since a first memory will be dedicated for CPU use and a second memory will be dedicated for peripheral use as shown in Figure 1A. The Examiner does not provide any rationale for adding (the limiting) aspects of the prior art system back into the very system that is supposed to remedy these limitations.

For completeness sake, and although the Examiner does not raise this point, it may be noted that the Luan system of Figure 2 shows multiple memory devices 104. These multiple memories do not teach Applicants' first and additional storage devices for at least the reason that each Luan memory device 104 provides a different portion of the Luan address space. Nothing in Luan teaches the possibility of retrieving the same data from more than one of these devices based on the state of programmable indicators.

Finally, an apparent alternative argument offered by the Examiner in the *Response to Arguments* section of the Final Rejection is considered. (See Final

Rejection p. 14.) There, the Examiner notes that Luan Fig. 4 shows memory configuration controller 202 coupled both to memory 104 and to a cache RAM 412, thereby teaching Applicants' first and second memories. However, nothing in Luan indicates the Luan memory configuration controller 202 uses any programmable mode to determine whether to retrieve requested data from cache 412, memory 104, or both, as claimed by Applicants' Claim 1.

Next, the Examiner's assertions regarding Chapin are considered. Claim 1 refers to "copies of the requested data" to convey the notion that the same data may be stored in Applicants' first and additional storage devices, a concept said to be taught by Chapin.

Chapin describes a mechanism for use with image reproduction systems (i.e., copiers.) The particular aspect of Chapin cited by the Examiner as teaching Applicants' data copies relates to the ability of the Chapin system to retrieve a copy of image data from system memory and display this data on a user interface 44 (e.g., a display screen) of a type shown in Chapin Fig. 2. (Final Rejection p. 9 in ref. to Chapin col. 13, lines 50-58.) This aspect does not teach Applicants' use of data copies stored in multiple storage devices. Moreover, Chapin does not add anything to Luan to teach any of the aspects of Applicants' invention discussed above in regards to Luan. Finally, one skilled in the art would not be motivated to incorporate aspects of the Chapin copier system into the Luan shared memory system. For at least the foregoing reasons, the current rejection of Claim 1 is improper. Likewise, the rejection of Claims 2-11 that depend from Claim 1 is also improper.

For brevity, only the independent Claims are discussed in detail herein. The various dependent Claims include additional aspects not taught or suggested by the cited references, as discussed in the response dated 2/16/06.

Respectfully submitted,

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